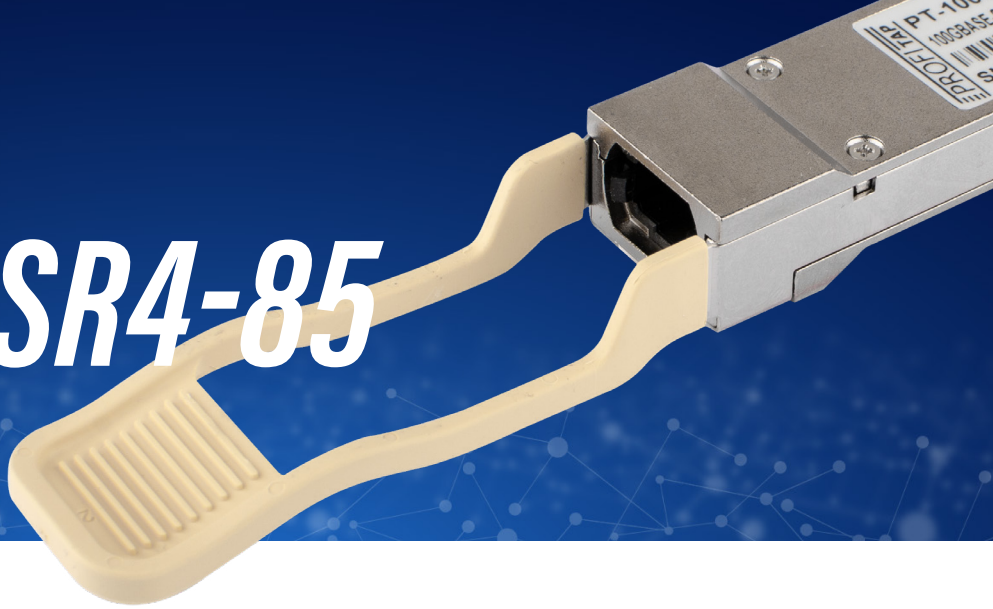


# PT-100G-SR4-85

## DATASHEET



### 1. PRODUCT FEATURES

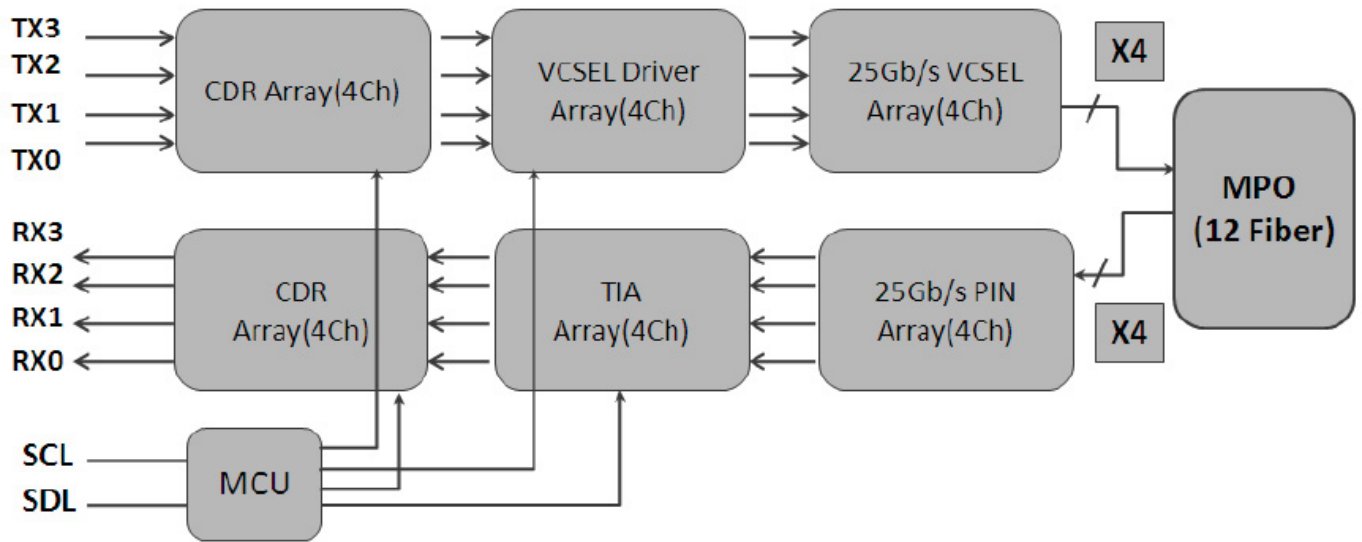
- ▶ 4 channels full-duplex transceiver modules.
- ▶ Transmission data rate up to 28.05Gbps per channel
- ▶ Compatible with 40GE and 56G FDR data rate
- ▶ 4 channels 850nm VCSEL array
- ▶ 4 channels PIN photo detector array
- ▶ Internal CDR circuits on both receiver and transmitter channels
- ▶ Support Electrical or Optical Loopbacks
- ▶ Low power consumption <3.5W
- ▶ Hot Pluggable QSFP form factor
- ▶ Maximum link length of 70m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF
- ▶ Single MPO connector receptacle
- ▶ Built-in digital diagnostic functions
- ▶ 3.3V power supply voltage
- ▶ RoHS 6 compliant (lead free)
- ▶ Operating case temperature  
Standard : 0 to +70°C  
Industrial : -40 to +85°C

### 2. GENERAL DESCRIPTION

Profitap PT-100G-SR4-85 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ SR4 for 100 or 40 Gigabit Ethernet and Infiniband FDR/EDR Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 104 Gbps bandwidth. Each lane can operate at 26Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses an 12 fiber MTP (MPO) connector. The PT-100G-SR4-85 provides reliable long life, high performance, and consistent service.

#### APPLICATIONS

- ▶ IEEE 802.3bm 100GBASE SR4 and 40GBASE SR4
- ▶ Infiniband FDR/EDR
- ▶ 128G Fibre Channel
- ▶ 4x28Gb/s Multimode OTN



### 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

### 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Min	Max	Unit
Supply Voltage	VCC	3.13	3.3	3.47	V
Case Operating Temperature	Tca	0		70	°C
Data Rate Per Lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			3.5	W
Fiber Bend Radius	Rb	3			cm

## 5. ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Min	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	$\Delta V_{in}$	300		1100	mVp-p
Differential output voltage amplitude	$\Delta V_{out}$	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			E-12	
Input Logic Level High	V <sub>IH</sub>	2.0		VCC	V
Input Logic Level Low	V <sub>IL</sub>	0		0.8	V
Output Logic Level High	V <sub>OH</sub>	VCC-0.5		VCC	V
Output Logic Level Low	V <sub>OL</sub>	0		0.4	V

### NOTE

1. BER=10<sup>-12</sup>; PRBS 2<sup>31</sup>-1@25.78125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

## 6. OPTICAL CHARACTERISTICS

### TRANSMITTER

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	$\lambda_c$	840	850	860	nm	
RMS spectral width	$\Delta\lambda$	-	-	0.6	nm	
Average launch power, each lane	P <sub>out</sub>	-8.4	-	2.4	dBm	
Optical Modulation Amplitude (OMA),each lane	OMA	-6.4		3	dBm	
Transmitter and dispersion eye closure(TDEC),each lane	TDEC			4.3	dB	
Extinction Ratio	ER	3	-	-	dB	
Average launch power of OFF transmitter, each lane				-30	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3						SPECIFICATION VALUES {0.3,0.38,0.45,0.35,0.41,0.5} Hit Ratio = 5x10 <sup>-5</sup>

### RECEIVER

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	$\lambda_c$	840	850	860	nm	
Stressed receiver sensitivity in OMA				-5.2	dBm	1
Maximum Average power at receiver, each lane				2.4	dBm	
Minimum Average power at receiver, each lane				-10.3	dBm	
Receiver Reflectance				-12	dB	
LOS Assert		-30			dBm	
LOS De-Assert – OMA				-7.5	dBm	
HyLOS steresis		0.5			dB	

#### NOTE

1. Measured with conformance test signal at TP3 for BER = 10e-12

## 7. PIN DEFINITION

<b>PIN</b>	<b>Logic</b>	<b>Symbol</b>	<b>Name / Description</b>	<b>Note</b>
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3 V Power supply receiver	2
11	LVC MOS-I	SCL	2-wire serial interface clock	
12	LVC MOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22		Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3 V Power supply transmitter	2
30		Vcc1	+3.3 V Power S	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

**NOTE**

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

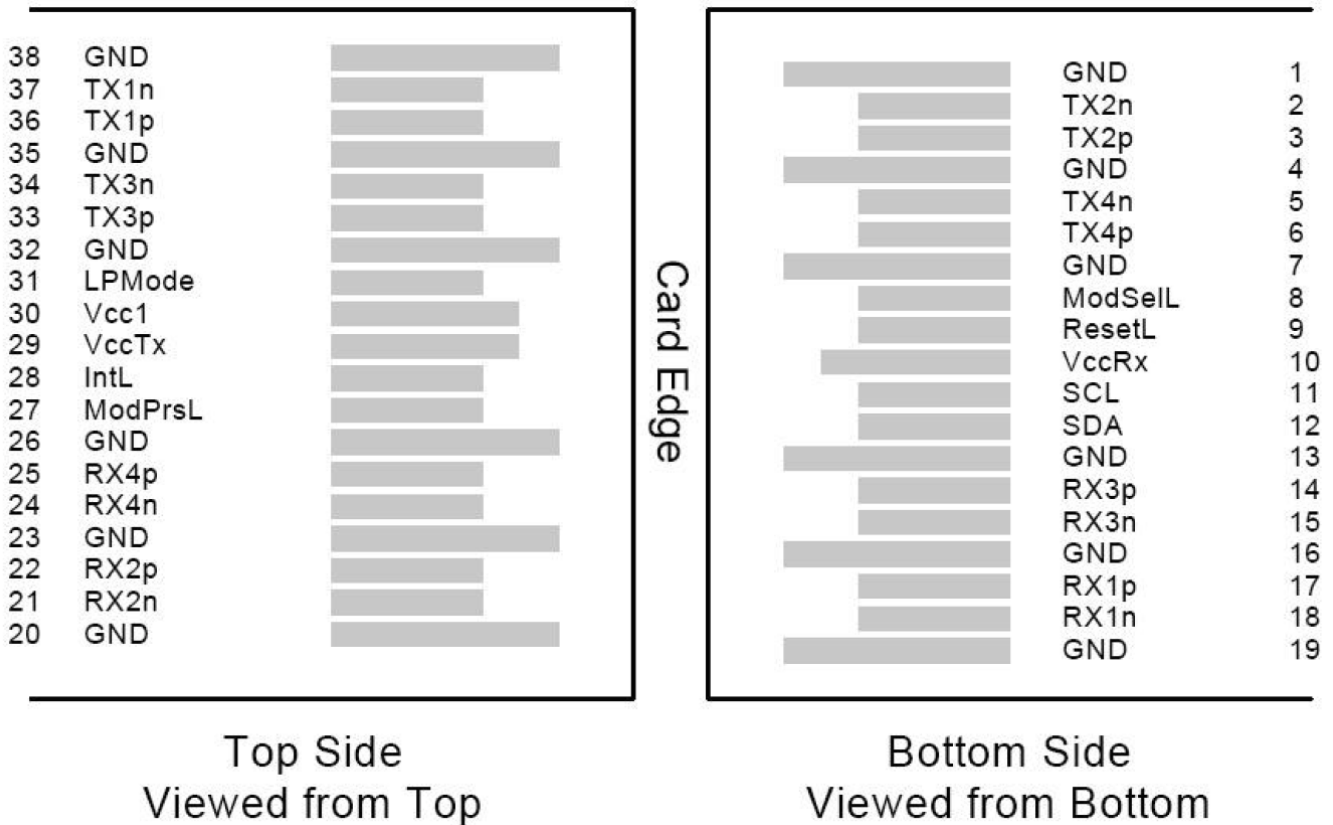


Figure 2. Electrical Pin-out Details

**ModSelL Pin**

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

**ResetL Pin**

Reset. LPMODE\_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t\_Reset\_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t\_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t\_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

**LPMode Pin**

Profitap PT-100G-SR4-85 operate in low power mode (less than 1.5 W power consumption). This pin active will decrease power consumption to less than 1W.

**ModPrsL Pin**

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

**IntL Pin**

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

### 8. POWER SUPPLY FILTERING

The host board should use the power supply filtering shown in Figure3.

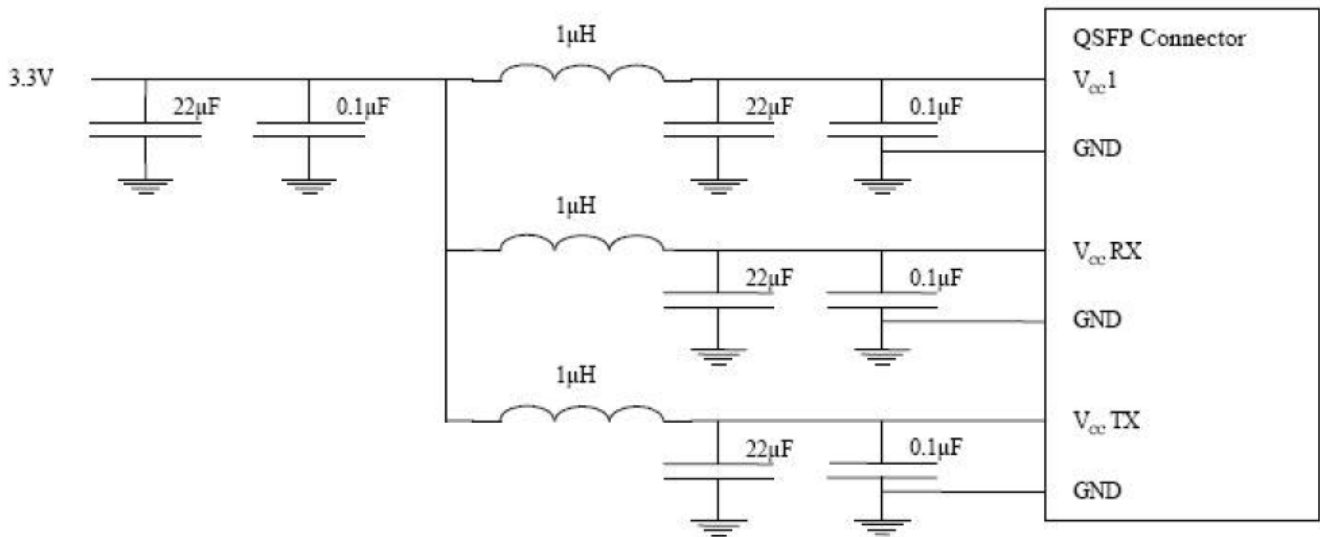
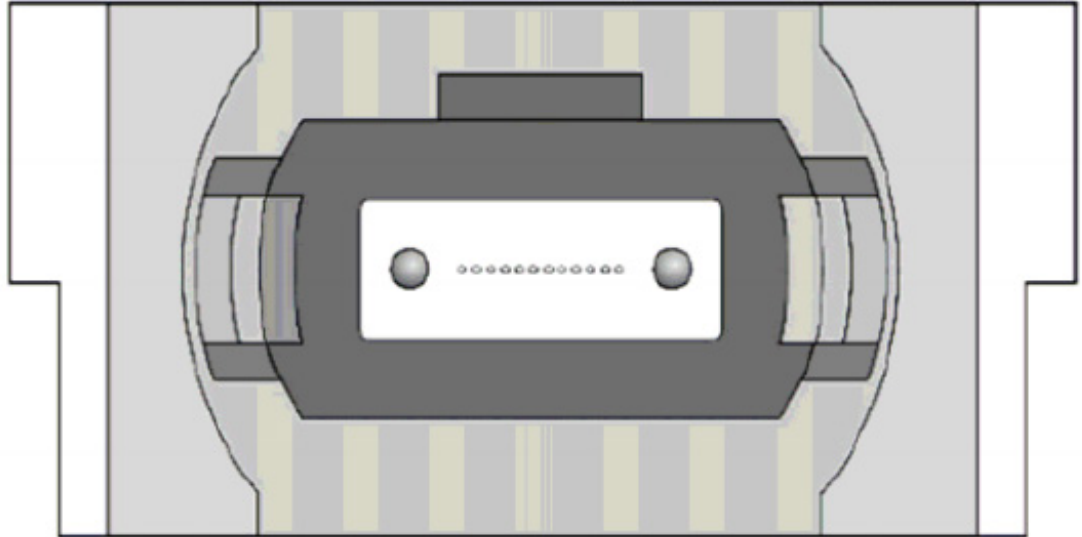


Figure 3. Host Board Power Supply Filtering

## 9. OPTICAL INTERFACE LANES AND ASSIGNMENT

The optical interface port is a male MPO connector. The four fiber positions on the left as shown in Figure 4, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.



Transmit Channels: 1 2 3 4  
Unused positions: X X X X  
Receive Channels: 4 3 2 1

Figure 4. Optical Receptacle and Channel Orientation



# 10. DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Profitap PT-100G-SR4-85. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

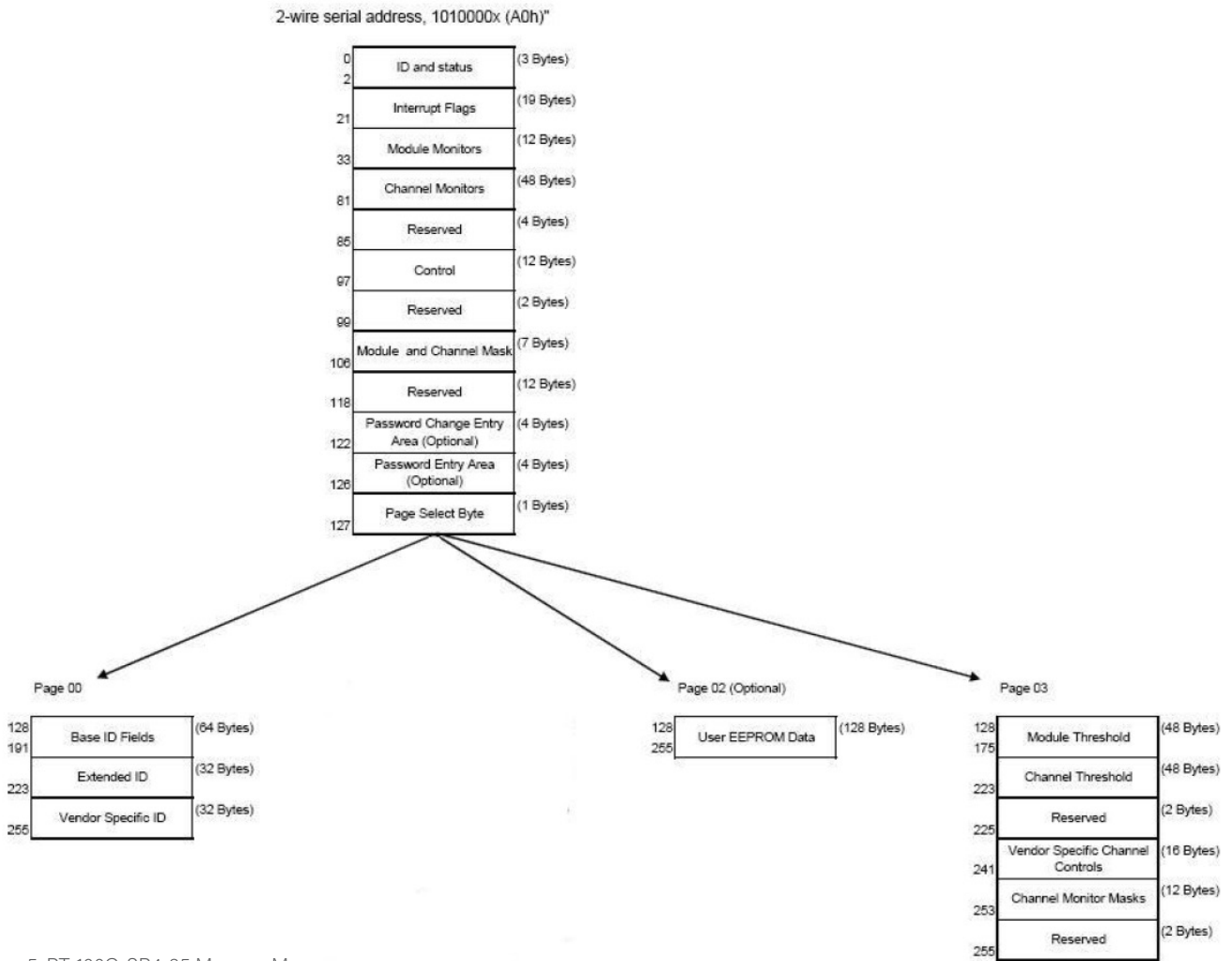


Figure 5. PT-100G-SR4-85 Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mb/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 $\mu\text{m}$ (1 Byte)	Link length supported for EBW 50/125 $\mu\text{m}$ fiber, units of 2 m
144	Length 50 $\mu\text{m}$ (1 Byte)	Link length supported for 50/125 $\mu\text{m}$ fiber, units of 1 m
145	Length 62.5 $\mu\text{m}$ (1 Byte)	Link length supported for 62.5/125 $\mu\text{m}$ fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand <sup>†</sup>
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 8. Page 00 Memory Map

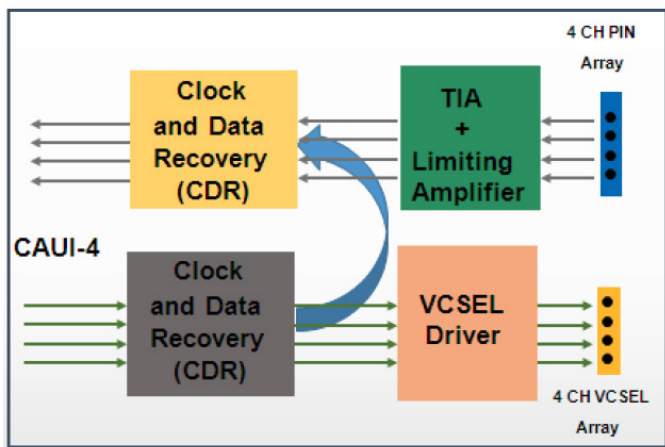
# 11. DEFINITIONS

## RATE SELECT

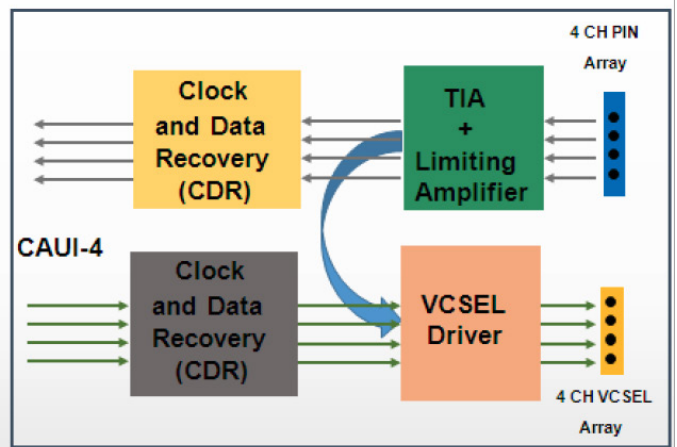
I2C Address 0xA0 Byte 0x6A(106)	
100GE/EDR/FDR	0x00 (default)
40GE	0x0B

## LOOPBACKS MODE SELECT

I2C Address 0xA0 Byte 0x69(105)	
Disable Loopbacks	0x00 (default)
Electrical Loopback	0x01
Optical Loopback	0x02



**Electrical Loopback Mode**



**Optical Loopback Mode**

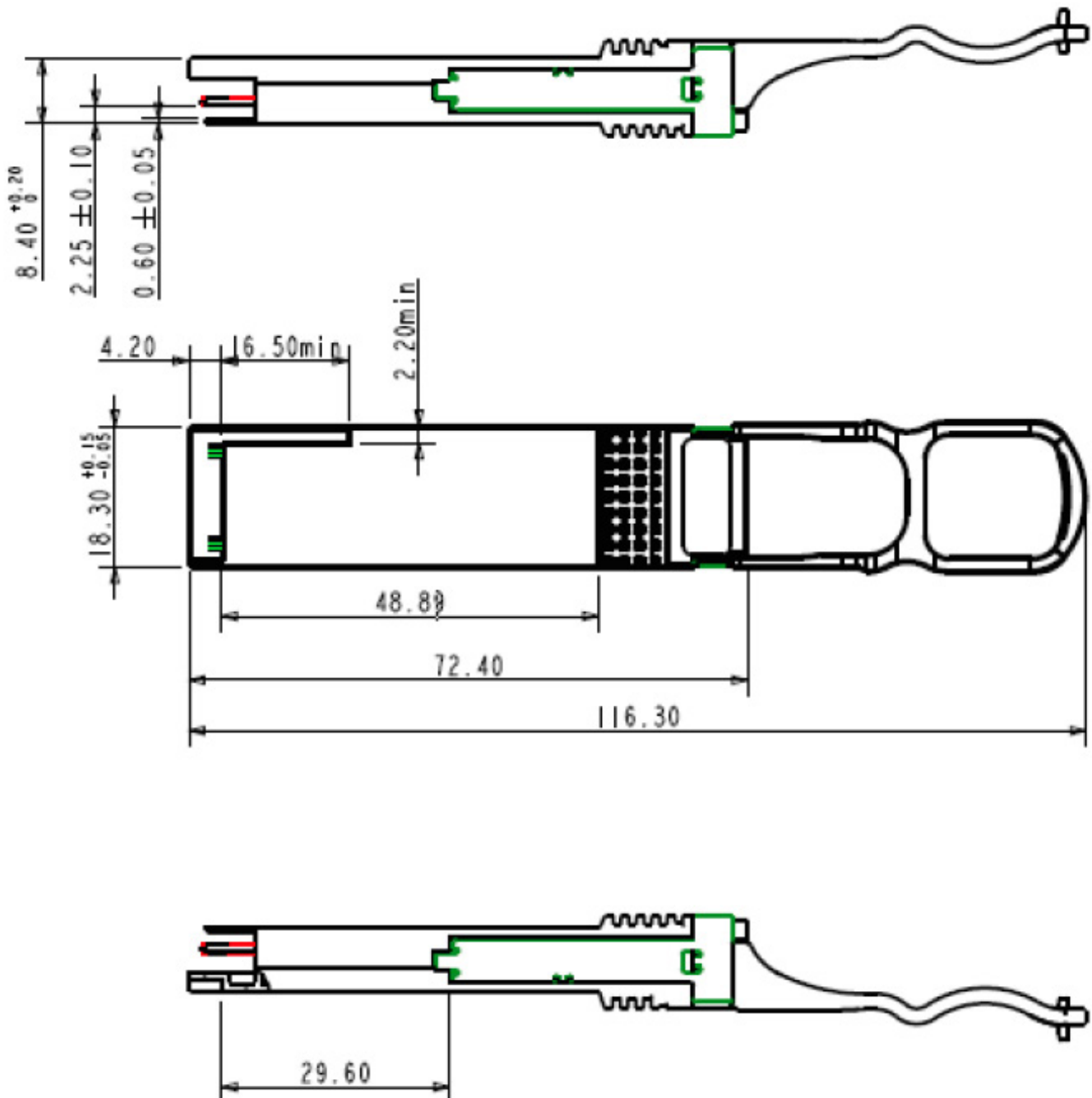
## 12. TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMMode Assert Time	ton_LPMMode	100	μs	Time from assertion of LPMMode (Vin:LPMMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

## NOTE

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

## 13. MECHANICAL DIMENSIONS



## 14. ORDERING INFORMATION

<i>Part Number</i>	<i>Product Description</i>
PT-100G-SR4-85	100GBASE-SR4 QSFP28 850NM 100M

### *IMPORTANT NOTICE*

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